IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A method for designing a cell-based application specific integrated circuit (ASIC) device, said method comprising:

reserving metal layer M1 for power supply bus when developing a bus structure of an ASIC device image;

grouping circuit macros of like power supply voltages into respective logic blocks;

synthesizing said logic blocks using sub-libraries corresponding to respective power supply voltages for said logic blocks; and

adding power supply bus for said power supply voltages to metal layer M1 in said logic blocks.

Please cancel Claim 2.

3. (original) The method of Claim 1, wherein one of said logic blocks contains a custom intellectual property macro.

4. (original) The method of Claim 1, wherein said method further includes utilizing a level convertor having multiple power supply voltages.

5. (currently amended) A computer program product residing on a computer usable medium for designing a cell-based application specific integrated circuit (ASIC) device, said computer program product comprising:

program code means for reserving metal layer M1 for power supply bus when developing a bus structure of an ASIC device image;

program code means for grouping circuit macros of like power supply voltages into respective logic blocks;

program code means for synthesizing said logic blocks using sub-libraries corresponding to respective power supply voltages for said logic blocks; and

program code means for adding power supply bus for said power supply voltages to metal layer M1 in said logic blocks.

Please cancel Claim 6.

7. (original) The computer program product of Claim 5, wherein one of said logic blocks contains a custom intellectual property macro.

8. (original) The computer program product of Claim 5, wherein said computer program product further includes program code means for utilizing a level convertor having multiple power supply voltages.

Please cancel Claims 9-12.